WHAT IS CLAIMED IS:

1. A silicon controlled rectifier comprising:

a first semiconductor material of a first conductivity type, the first semiconductor material having a top surface;

a second semiconductor material of a second conductivity type formed on the first semiconductor material, the second semiconductor material having a top surface and a dopant concentration;

a first semiconductor region of the first conductivity type formed in the second semiconductor material, the first semiconductor region contacting the top surface of the second semiconductor material;

a second semiconductor region of the second conductivity type formed in the second semiconductor material;

a third semiconductor region of the first conductivity type formed in the second semiconductor material, the second semiconductor region lying between and spaced apart from the first and third semiconductor regions; and

a fourth semiconductor region of the second conductivity type formed in the second semiconductor material, the first, second, third, and fourth semiconductor regions being spaced apart from each other.

2. The silicon controlled rectifier of claim 1 wherein the third semiconductor region extends from the top surface of the second semiconductor material to the top surface of the first semiconductor material.

3. The silicon controlled rectifier of claim 2 wherein the fourth semiconductor region extends from the top surface of the second semiconductor material to the first semiconductor material.

4. The silicon controlled rectifier of claim 3 wherein the second semiconductor region includes:

a first highly doped region that contacts the top surface of the second semiconductor material; and

a second highly doped region that lies below the first highly doped region, the first and second highly doped regions being spaced apart by a region having a lower dopant concentration.

5. The silicon controlled rectifier of claim 4 wherein the fourth semiconductor region includes:

a third highly doped region that contacts the surface of the second semiconductor material; and

a fourth highly doped region that lies below the third highly doped region, the third and fourth highly doped regions being spaced apart by a region having a lower dopant concentration.

6. The silicon controlled rectifier of claim 5 wherein the third semiconductor region includes a plurality of dopant concentration regions that lie between the top surface of the second semiconductor material and the top surface of the first semiconductor material.

7. The silicon controlled rectifier of claim 6 wherein the plurality of dopant concentrations continually decrease when moving from the top surface of the second semiconductor material to the top surface of the first semiconductor material.

8. The silicon controlled rectifier of claim 6 wherein the plurality of dopant concentrations decrease and then increase when

moving from the top surface of the second semiconductor material to the top surface of the first semiconductor material.

9. The silicon controlled rectifier of claim 6 and further comprising:

a layer of isolation material formed on the second semiconductor material, the layer of isolation material having a plurality of openings that expose the first, third, and fourth semiconductor regions;

a first conductive region formed on the isolation material that makes an electrical connection with the first semiconductor region;

a second conductive region formed on the isolation material that makes an electrical connection with the third semiconductor region; and

a third conductive region formed on the isolation material that makes an electrical connection with the fourth semiconductor region.

10. The silicon controlled rectifier of claim 9 and further comprising a fifth conductive region that contacts the first conductive region, and wherein the fifth conductive region extends laterally over the second semiconductor material from the second semiconductor region towards the third semiconductor region a distance to limit charge carriers from flowing between the second and third semiconductor regions along the top surface of the second semiconductor material.

11. The silicon controlled rectifier of claim 10 and further comprising a sixth conductive region that contacts the second and third conductive regions.

12. The silicon controlled rectifier of claim 9 wherein the layer of isolation material includes an opening that exposes the second

semiconductor region, a fourth conductive region making an electrical connection with the second semiconductor region.

13. The silicon controlled rectifier of claim 12 and further comprising a fifth conductive region that contacts the first and fourth conductive regions, and wherein the fifth conductive region extends laterally over the second semiconductor material from the second semiconductor region towards the third semiconductor region a distance to limit charge carriers from flowing between the second and third semiconductor regions along the top surface of the second semiconductor material.

14. The silicon controlled rectifier of claim 13 and further comprising a sixth conductive region that contacts the second and third conductive regions.

15. The silicon controlled rectifier of claim 1 wherein the third semiconductor region includes a plurality of dopant concentration regions that lie between the top surface of the second semiconductor material and the top surface of the first semiconductor material.

16. The silicon controlled rectifier of claim 15 wherein the plurality of dopant concentrations continually decrease when moving from the top surface of the second semiconductor material to the top surface of the first semiconductor material.

17. The silicon controlled rectifier of claim 16 wherein the plurality of dopant concentrations decrease and then increase when

moving from the top surface of the second semiconductor material to the top surface of the first semiconductor material.

18. The silicon controlled rectifier of claim 17 and further comprising:

a layer of isolation material formed on the second semiconductor material, the layer of isolation material having a plurality of openings that expose the first, third, and fourth semiconductor regions;

a first conductive region formed on the isolation material that makes an electrical connection with the first semiconductor region;

a second conductive region formed on the isolation material that makes an electrical connection with the third semiconductor region; and

a third conductive region formed on the isolation material that makes an electrical connection with the fourth semiconductor region.

19. The silicon controlled rectifier of claim 18 wherein the second and third conductive regions are electrically connected together.

20. A method of forming a silicon controlled rectifier, the method comprising the steps of:

forming a first semiconductor material of a first conductivity type, the first semiconductor material having a top surface;

forming a second semiconductor material of a second conductivity type on the first semiconductor material, the second semiconductor material having a top surface and a dopant concentration;

forming spaced-apart first and second semiconductor regions of the first conductivity type in the second semiconductor material; and

forming spaced-apart third and fourth semiconductor regions of a second conductivity type in the second semiconductor material, the third semiconductor region lying between and spaced apart from the first and second semiconductor regions.

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